Stable and Uniform InAlAs/InGaAs HEMT ICs for 40 Gbit/s Optical Communication Systems

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We developed thermally stable InAlAs/InGaAs HEMTs which have uniform offset-voltage in differential pairs of FETs. The standard deviation (σ) of offset-voltage is 8 mV. The HEMTs also indicate a small change of V_{th} within 11 mV under the annealing temperature of 330℃. These properties are essential for the operation of 40 Gbit/s optical communication circuits.

Fig. 1 shows the cross-section of an InAlAs/InGaAs HEMT. We performed an electron-beam lithography technique for a gate and a recess fabrication process. An InP stop layer is employed to control the depth of recess etching. We used wet chemical etching for the recess resulting in a highly uniform V_{th} and less damage in the carrier supply layer. The recess region is covered with thin SiN dielectric film using a plasma-enhanced CVD system. A gate electrode consisting of Ti/Pt/Au is evaporated on the InP layer and lifted off. The gate length is 0.13 μm. We introduced double-layer interconnection using benzocyclobutene (BCB) inter-layer dielectric film.

The average value of transconductance (gm) is 917 mS/mm and the standard deviation is 15 mS/mm. The cutoff frequency (f_T) is 175 GHz.

Fig. 2 shows the histogram for the V_{th} of the HEMTs fabricated on a 3-inch wafer. The average value is –0.63 V. The standard deviation is 13 mV, indicating better fabrication uniformity of the gate and the recess region than reported[1)]. Fig. 3 shows the histogram for the offset-voltage in differential pairs of FETs which consist of several wafers in deferent lot. We obtained a small standard deviation of 8 mV in the offset-voltage among them that indicates InP HEMTs are available for ICs which consist of source-coupled FET logic (SCFL).

Thermal stability is important for operating the ICs. Fig. 4 shows the dependence of the V_{th} on annealing time. A small change of only 11 mV occurred through 60 minutes of annealing under the temperature of 330℃. Fig. 5 shows change in gm and Ids before and after annealing at 330℃. We observed less change in the gm and Ids. This indicates that the InAlAs/InGaAs HEMTs are thermally stable in practical use due to the good gate-electrode property. Furthermore, we believe that it is essential to passivate the InP etch-stop layer on the recess region entirely using the dielectric film.

In conclusion, we fabricated thermally stable and V_{th} uniform InAlAs/InGaAs HEMTs. They showed less change in V_{th} under the annealing temperature of 330℃ and uniform V_{th} which has the standard deviation of 13 mV. These results suggest that InP-based HEMTs with the recess covered with an InP layer are essential for the thermally stable operation of 40 Gbit/s optical communication circuits.

1) T. Suemitsu, et al., Improved recessed-gate structure for sub-0.1-μm-gate InP-based high electron mobility transistors, Jpn. J. Appl. Phys. Vol.37(1998) pp.1365-1372

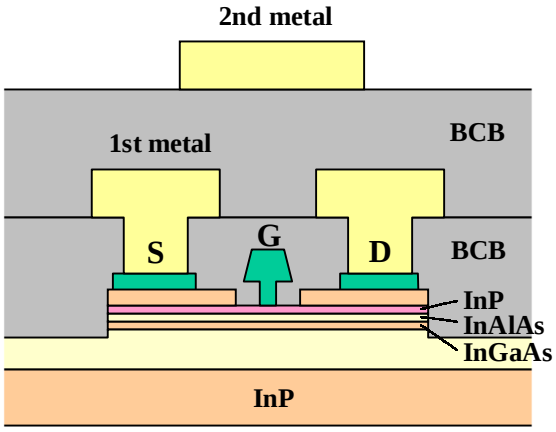

Fig. 1 Cross-section of an InAlAs/InGaAs HEMT.

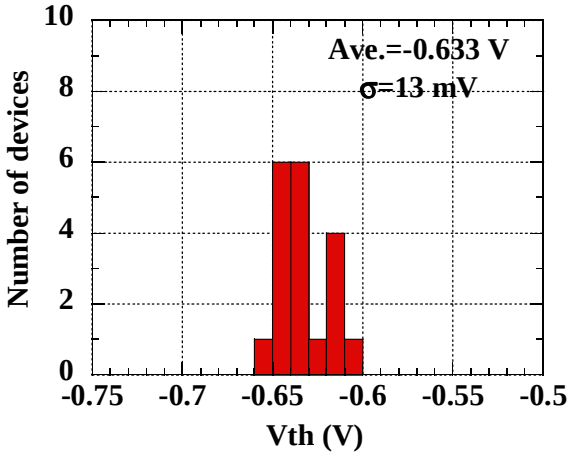

Fig. 2 Histogram of threshold voltage.

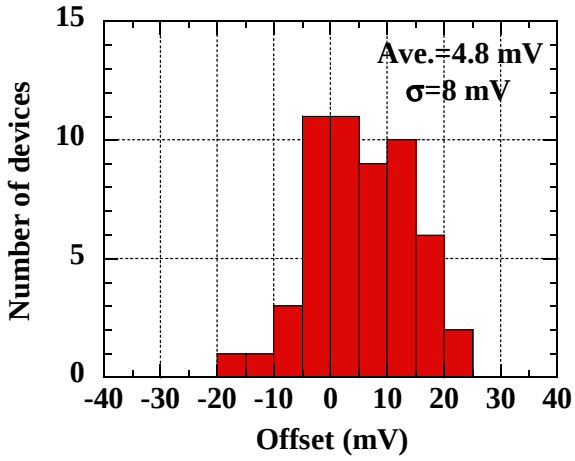

Fig. 3 Histogram for the offset voltage in differential pairs of FETs.

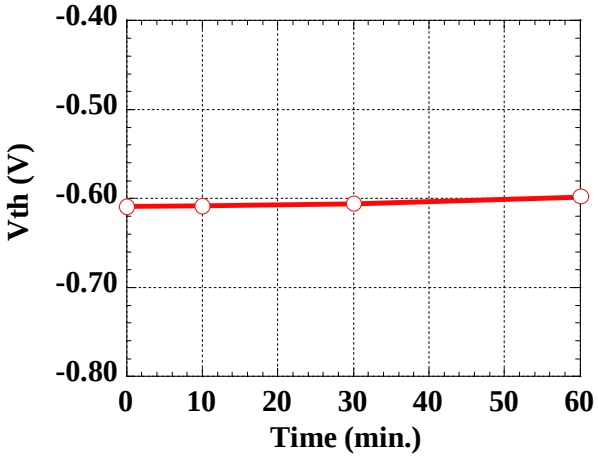

Fig. 4 Vth dependence on annealing time.

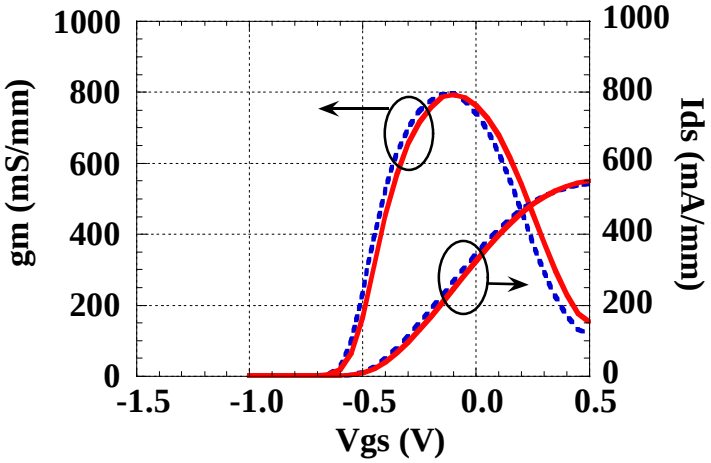

Fig.5 Change in gm and Ids before (broken line) and after (solid line) the annealing at 330℃.